Notice of Allowability	Application No.	Applicant(s)	
	09/852,009	REED, COKE S.	
	Examiner	Art Unit	
	Brian D. Nguyen	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/3/06*.

2. ☒ The allowed claim(s) is/are *39-40 and 42-116 (renumbered 1-77, respectively)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *01102006* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1/11/06

BRIAN NGUYEN
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Ken J. Koestner on 1/10/06.

3. The claims have been amended as follows:

39. (Currently Amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with each device in the device set A being capable of sending data to a node in the node set T;

a device set Z mutually exclusive of the node set T with each device in the device set Z being capable of receiving data from a node in the node set T;

a collection C of node sets that are subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C;

for a device x in the device set Z, a sequence $cx = cx_o, cx_1, cx_2,..., cx_J$ exists with each member of the sequence cx being a node set in the collection C, the sequence cx being capable of passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is in a member of the sequence cx, a node of the path R that receives a message

directly from a device in the device set A being in a set having ~~the~~ a form cx_u and a node of the path R that sends data directly to the device x being in a set of ~~the~~ a form cx_v with U being larger than V;

for a member Q of the collection C, a corresponding set of devices Z(Q) exists in the device set Z such that a device ~~q~~ zq is included in the set of devices Z(Q) only if the member Q is also a member of a sequence cq;

for members CXH and CXK of the sequence cx with H > K, a device set Z(cx_K) is a subset of a device set Z(cx_H) and a device exists in the device set Z(cx_H) that is not included in the device set Z(cx_K); and

the node set T includes three distinct nodes p, q, and r, the node p being in a member cz_D of a sequence cz, the nodes q and r being in a member cz_E of the sequence cz with D > E, in one path of ~~paths~~ path set P(x) a message moves directly from the node p to the node r and in another path of ~~paths~~ path set P(x) a message moves directly from the node q to the node r.

40. (Currently Amended): An interconnect structure according to Claim 39 wherein:

~~paths P(x) include~~ the path set P(x) includes a path such that if a message hops from a node in a member cz_n to a node in a member cz_m, then ~~n ≥: m~~ $n \geq m$.

41. (Cancelled).

43. (Currently Amended): An interconnect structure according to claim 42 wherein:

a message M_y targeted for a device y in the device set Z enters at a node on the level L_J and exits at an output port on the level L_0 with the output port being connected to the device y; and

for a hop in a path of the message M_y from a node of a level L_U to a node of a level L_V, U being greater than or equal to V.

44. (Currently Amended): An interconnect structure according to claim 43 wherein:

the collection C includes 2^{J-N} members on a level ~~N~~ L_N;

the collection C includes three ~~members~~ member node sets D, E and F such that the member node set D is on the level L_N and member node sets E and F are on a level L_{N-1};

the interconnect set I includes interconnects positioned to allow data to pass directly from the member node set D to the member node set E and to pass directly from the node set D to the node set F; and

the device set Z includes device sets Z(D), Z(E), and Z(F) that correspond to the three ~~members~~ member node sets D, E, and F, the device sets Z(E) and Z(F) being mutually exclusive device sets, and the device set Z(D) is the union of the device sets Z(E) and Z(F).

46. (Currently Amended): An interconnect structure in accordance with Claim 39 further comprising:

a logic L_p associated with the node p wherein for a message Mp that arrives at the node p, the logic ~~Lp~~ L_p uses information concerning the sending of messages from the node q for the logic ~~Lp~~ L_p to determine where the node p is to send the message Mp.

47. (Currently Amended): An interconnect structure according to claim 46 wherein:

the node q has priority over the node p to send data to the node r so that a message Mq located at the node q is not blocked from being sent to the node r by ~~a~~ the message Mp at the node p.

51. (Currently Amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with each device in the device set A being capable of sending data to a node in the node set T;

a device set Z mutually exclusive of the node set T with each device in the device set Z being capable of receiving data from a node in the node set T;

a collection C of node sets that are subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C;

for a device x in the device set Z, a sequence $cx = cx_0, cx_1, cx_2, ..., cx_J$ exists with each member of the sequence cx being a node set in the collection C, the sequence cx being capable of passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is in a member of the sequence cx, a node of the path R that receives a message directly from a device in the device set A being in a set having ~~the~~ a form cx_U and a node of the path R that sends data directly to the device x being in a set of ~~the~~ a form cx_V with U being larger than V;

for a member Q of the collection C, a corresponding set of devices Z(Q) exists in the device set Z such that a device q is included in the set of devices Z(Q) only if the member Q is also a member of a sequence cq;

for members cx_H and cx_K of the sequence cx with $H > K$, a device set $Z(cx_K)$ is a subset of a device set $Z(cx_H)$ and a device exists in the device set $Z(cx_H)$ that is not included in the device set $Z(cx_K)$; and

the node set T includes three distinct nodes p, q, and r, the nodes p and q being in a member cz_D of sequence cz, the node r being in a member cz_E of the sequence cz with $D > E$, in a first path of ~~paths~~ path set P(x) a message moves directly from the node p to the node q, in a second path of ~~paths~~ path set P(x) a message moves directly from the node p to the node r.

52. (Currently Amended): An interconnect structure according to Claim 51 wherein:

~~paths P(x) include~~ the path set P(x) includes a path such that if a message hops from a node in a member cz_n to a node in a member cz_m, then $n \geq m$.

53. (Currently Amended): An interconnect structure according to Claim 51 further comprising:

an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets $L = L_0, L_1, \ldots L_J$ each member of the hierarchy L being a node set that is subset of the node set T and each node in the node set T is contained in exactly one member of the node set L; and

for the device x of the device set Z, a member node set cz_N is a subset of a level N node set L_N, N not exceeding J.

54. (Currently Amended): An interconnect structure according to Claim 53 wherein:

a message M_y targeted for a device y in the device set Z enters at a node on the level L_J and exits at an output port on the level L_0 with the output port being connected to the device y; and

for a hop in a path of the message M_y from a node of a level L_U to a node of a level L_V, U being greater than or equal to V.

55. (Currently Amended): An interconnect structure according to Claim 54 wherein:

the collection C includes 2^{J-N} members on a level N;

the collection C includes three ~~members~~ member node sets D, E and F such that the member node set D is on the level L_N and member node sets E and F are on a level L_{N-1};

the interconnect set I includes interconnects positioned to allow data to pass directly from the member node set D to the member node set E and to pass directly from the member node set D to the member node set F; and

the device set Z includes device sets Z(D), Z(E), and Z(F) that correspond to the three ~~members~~ member node sets D, E, and F, the device sets Z(E) and Z(F) being mutually exclusive device sets, and the device set Z(D) is the union of the device sets Z(E) and Z(F).

59. (Currently Amended): An interconnect structure according to Claim 57 wherein:

a node N_U of the node set ~~p~~ P is not blocked from sending data to the node N_E as a result of data sent to the node N_E from a node N_V having a priority lower than the node N_U for sending data to ~~the.~~ the node N_E.

62. (Currently Amended): An interconnect structure according to Claim 57 further comprising:

the plurality of nodes including the node N_F, the node N_A, and a node set R, the nodes N_F and ~~NA~~ N_A being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

a plurality of control interconnect paths coupling the plurality of nodes, the control interconnect paths used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to a logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set R the node N_A sends data.

63. (Currently Amended): An interconnect structure according to Claim 57 wherein:

the plurality of nodes include the nodes N_A, N_E, and N_F, and a node N_D;

the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of interconnect paths further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect

path for sending a control signal from a source associated with the node N_F to a logic element L_A associated with the node N_A, and

for ~~a~~ the message M arriving at the node N_F, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

64. (Currently Amended): An interconnect structure according to Claim 57 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes N_F, N_A, N_E, and N_D;

the plurality of ~~data-carrying~~ data interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

a plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route ~~a~~ the message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

66. (Currently Amended): An interconnect structure according to Claim 57 further comprising:

one or more output ports in which an output port that is accessible from the node N_A is not accessible from the node ~~N_E~~ N_E.

75. (Currently Amended): An interconnect structure according to Claim 68 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes N_F, N_A, N_E, and N_D;

the plurality of data interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

a plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a the message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

78. (Currently Amended): An interconnect structure according to Claim 68 further comprising:

the distinct nodes N_A and N_F of the plurality of nodes;

means for sending a plurality of messages including a the message M_A and a the message M_F through the interconnect structure nodes, the message M_F including one or more header bits;

means for routing the message M_F to enter the node N_F of the interconnect structure;

means for routing the message M_A to enter the node N_A of the interconnect structure; and

means for using header bits of the message M_F at the node N_F to route the message M_A from the node N_A.

96. (Previously Presented): An interconnect structure according to Claim 79 further comprising:

a node ~~distinct nodes N_A and~~ N_F of the plurality of nodes distinct from the node N_A;

means for sending a plurality of messages including a message M_A and a message M_F through the interconnect structure nodes, the message M_F including one or more header bits;

means for routing the message M_F to enter the node N_F of the interconnect structure;

means for routing the message M_A to enter the node N_A of the interconnect structure; and

means for using header bits of the message M_F at the node N_F to route the message M_A from the node N_A.

104. (Currently Amended): An interconnect structure according to Claim 98 further comprising:

the plurality of nodes including a node N_F and a node set R, the nodes N_F and N_A being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

a plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, and

the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to ~~the~~ a logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set R the node N_A sends data.

107. (Currently Amended): An interconnect structure according to Claim 98 wherein:

the plurality of nodes include a node N_F;

the plurality of interconnects include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control- signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of ~~plurality of~~ interconnects further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to a logic element L_A associated with the node N_A, and

for a message M arriving at the node N_F, a source associated with the node N_F sends a control signal ~~S~~ s to the logic element L_A, the logic element L_A using the control signal ~~S~~ s to determine between sending the message M to the node N_E or to the node N_D.

108. (Currently Amended): An interconnect structure according to Claim 107 wherein:

a message M' arriving at the node N_A is routed to a node N_Z distinct from the nodes N_E, N_D, and N_F.

111. (Currently Amended): An interconnect structure according to Claim 98 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including a node N_F, the nodes N_F, N_A, N_E, and N_D being mutually distinct;

a plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

a plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal ~~S~~ s received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal ~~S'~~ s' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

113. (Currently Amended): An interconnect structure according to Claim 111 wherein:

routing of a message M' passing through the node N_A is the same whether the control signal from the node N_F is the control signal ~~S~~ s or the control signal ~~S'~~ s'.

115. (Currently Amended): An interconnect structure according to Claim 98 further comprising:

a node ~~distinct nodes N_A and~~ N_F of the plurality of nodes distinct from the node N_A;

means for sending a plurality of messages including a message M_A and a message M_F through the interconnect structure nodes, the message M_F including one or more header bits;

means for routing the message M_F to enter the node N_F of the interconnect structure;

means for routing the message M_A to enter the node N_A of the interconnect structure; and

means for using header bits of the message M_F at the node N_F to route the message M_A from the node N_A.~~30.~~

Allowable Subject Matter

4. The following is an examiner's statement of reasons for allowance:

Regarding claims 39-40, 42-56, and 79-116, the prior art of record fails to teach a device set A mutually exclusive of the node set T with each device in the device set A being capable of sending data to a node in the node set T; a device set Z mutually exclusive of the node set T with each device in the device set Z being capable of receiving data from a node in the node set T; a

collection C of node sets that are subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C.

Regarding claims 57-78, the prior art of record fails to teach the nodes in the node set P having a priority relationship for sending data to the node N_E, the nodes in the node set P including distinct nodes N_F and N_A, the node N_F having a highest priority among the nodes in the node set P for sending data to the node N_E so that a message M_F arriving at the node N_F is not blocked from traveling to the node N_E by a message M_A arriving at the node N_A.

Conclusion

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian D. Nguyen whose telephone number is (571) 272-3084. The examiner can normally be reached on 7:30-6:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/11/06

BRIAN NGUYEN
PRIMARY EXAMINER